WHAT IS CLAIMED IS:

1. A data transfer system comprising:

a channel;

a transmission unit comprising

a first host adapted to transmit parallel data and a first clock signal, and

a serialization unit comprising

a buffer adapted to receive the parallel data from the serialization unit according to the first clock signal, and to transmit the parallel data according to a second clock signal, wherein the buffer comprises a plurality of storage cells adapted to store the parallel data received by the buffer,

a buffer controller adapted to cause the buffer to transmit an additional predetermined amount of the parallel data when a number of the storage cells storing the parallel data received by the buffer but not yet transmitted by the buffer is less than or equal to a first threshold;

wherein the buffer controller is further adapted to cause the buffer to delete a predetermined amount of the parallel data when a number of the storage cells storing the parallel data received by the buffer but not yet transmitted by the buffer is greater than or equal to a second threshold.

and

a serializer adapted to convert the parallel data transmitted by the buffer to serial data, and to transmit the serial data to the channel according to the second clock signal,

wherein the first and second clock signals are independent; and

a reception unit comprising

a deserialization unit comprising

a deserializer adapted to receive the serial data from the channel, and

to convert the serial data to the parallel data, and

a second host adapted to receive the parallel data from the deserialization unit.

2. The data transfer system of claim 1:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined additional amount of the parallel data comprises one of the fill words.

3. The data transfer system of claim 1:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the parallel data that is deleted by the buffer comprises one of the fill words.

4. The data transfer system of claim 1:

wherein the buffer comprises a plurality of storage cells adapted to store the parallel data received by the buffer;

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

5. The data transfer system of claim 1:

wherein the buffer comprises a plurality of storage cells adapted to store the parallel data received by the buffer;

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

6. The data transfer system of claim 1, wherein the buffer is a first-in first-out (FIFO) buffer.

7. The data transfer system of claim 1, wherein the channel comprises a fibre channel.

8. The data transfer system of claim 1, wherein the serializer is further adapted to transmit the serial data to the channel at a rate greater than or equal to 4 Gbps.

9. A storage area network (SAN) comprising the data transfer system of claim 1.

10. A data transfer system comprising:

channel means for transferring data;

transmission means for transmitting the data, the transmission means comprising

first host means for transmitting parallel data and a first clock signal, and

serialization means for serializing the data, the serialization means comprising

buffer means for receiving the parallel data from the serialization means according to the first clock signal, and for transmitting the parallel data according to a second clock signal, wherein the buffer means comprises a plurality of storage cell means for storing the words of the digital data received by the buffer means,

buffer controller means for causing the buffer means to transmit an additional predetermined amount of the parallel data when a number of the storage cell means storing the parallel data received by the buffer means but not yet transmitted by the buffer means is less than or equal to a first threshold;

wherein the buffer controller means causes the buffer means to delete a predetermined amount of the parallel data when a number of the storage cell means storing the parallel data received by the buffer means but not yet transmitted by the buffer means is greater than or equal to a second threshold.

serializer means for converting the parallel data transmitted by the buffer means to serial data, and to transmit the serial data to the channel means according to the second clock signal,

wherein the first and second clock signals are independent; and

reception means for receiving the data, the reception means comprising

deserialization means for deserializing the data, the deserialization means comprising

deserializer means for receiving the serial data from the channel means, and for converting the serial data to the parallel data, and

second host means for receiving the parallel data from the deserialization means.

11. The data transfer system of claim 10:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the parallel data comprises one of the fill words.

12. The data transfer system of claim 10:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the parallel data that is deleted by the buffer means comprises one of the fill words.

13. The data transfer system of claim 10:

wherein the buffer means comprises a plurality of storage cell means for storing the parallel data received by the buffer means;

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

14. The data transfer system of claim 10:

wherein the buffer means comprises a plurality of storage cell means for storing the parallel data received by the buffer means;

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

15. The data transfer system of claim 10, wherein the serializer means transmits the serial data to the channel at a rate greater than or equal to 4 Gbps.

16. A storage area network (SAN) comprising the data transfer system of claim 10.

17. A data transceiver comprising:

a host adapted to receive first parallel data, and to transmit second parallel data and a first clock signal; and

a serializer/deserializer (SERDES) comprising

a deserialization unit comprising

a deserializer adapted to receive first serial data from a channel, and to convert the first serial data to the first parallel data, and

a serialization unit comprising

a buffer adapted to receive the second parallel data according to the first clock signal, and to transmit the second parallel data according to a second clock signal, wherein the buffer comprises a plurality of storage cells adapted to store the second parallel data received by the buffer,

a buffer controller adapted to cause the buffer to transmit an additional predetermined amount of the second parallel data when a number of the storage cells storing the second parallel data received by the buffer but not yet transmitted by the buffer is less than or equal to a first threshold;

wherein the buffer controller is further adapted to cause the buffer to delete a predetermined amount of the second parallel data when a number of the storage cells storing the second parallel data received by the buffer but not yet transmitted by the buffer is greater than or equal to a second threshold, and

a serializer adapted to convert the second parallel data transmitted by the buffer to second serial data, and to transmit the second serial data to the channel according to the second clock signal,

wherein the first and second clock signals are independent.

18. The data transceiver of claim 17:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the second parallel data comprises one of the fill words.

19. The data transceiver of claim 17:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the second parallel data that is deleted by the buffer comprises one of the fill words.

20. The data transceiver of claim 17:

wherein the buffer comprises a plurality of storage cells adapted to store the second parallel data received by the buffer;

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

21. The data transceiver of claim 17:

wherein the buffer comprises a plurality of storage cells adapted to store the second parallel data received by the buffer;

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

22. The data transceiver of claim 17, wherein the buffer is a first-in first-out (FIFO) buffer.

23. The data transceiver of claim 17, wherein the channel comprises a fibre channel.

24. The data transceiver system of claim 17, wherein the serializer is further adapted to transmit the serial data to the channel at a rate greater than or equal to 4 Gbps.

25. A storage area network (SAN) comprising the data transceiver of claim 17.

26. A data transceiver comprising:

host means for receiving first parallel data, and for transmitting second parallel data and a first clock signal; and

serializer/deserializer (SERDES) means for serializing and deserializing the data, the SERDES means comprising

deserialization means for deserializing the data, the deserialization means comprising

deserializer means for receiving first serial data from a channel, and for converting the first serial data to the first parallel data, and

serialization means for serializing the data, the serialization means comprising

buffer means for receiving the second parallel data according to the first clock signal, and for transmitting the second parallel data according to a second clock signal, wherein the buffer means comprises a plurality of storage cell means for storing the second parallel data received by the buffer means,

buffer controller means for causing the buffer means to transmit an additional predetermined amount of the second parallel data when a number of the storage cell means storing the second parallel data received by the buffer means but not yet transmitted by the buffer means is less than or equal to a first threshold;

wherein the buffer controller means causes the buffer means to delete a predetermined amount of the second parallel data when a number of the storage cell means storing the second parallel data received by the buffer means but not yet transmitted by the buffer means is greater than or equal to a second threshold, and

serializer means for converting the second parallel data transmitted by the buffer means to second serial data, and for transmitting the second serial data to the channel according to the second clock signal,

wherein the first and second clock signals are independent.

27. The data transceiver of claim 26:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the second parallel data comprises one of the fill words.

28. The data transceiver of claim 26:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the second parallel data that is deleted by the buffer means comprises one of the fill words.

29. The data transceiver of claim 26:

wherein the buffer means comprises a plurality of storage cell means for storing the second parallel data received by the buffer means;

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

30. The data transceiver of claim 26:

wherein the buffer means comprises a plurality of storage cell means for storing the second parallel data received by the buffer means;

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

31. The data transceiver of claim 26, wherein the serializer means transmits the serial data to the channel at a rate greater than or equal to 4 Gbps.

32. A storage area network (SAN) comprising the data transceiver of claim 26.

33. A serializer/deserializer (SERDES) comprising:

a deserialization unit comprising

a deserializer adapted to receive first serial data from a channel, and to convert the first serial data to first parallel data; and

a serialization unit comprising

a buffer adapted to receive second parallel data according to a first clock signal, and to transmit the second parallel data according to a second clock signal,

wherein the buffer comprises a plurality of storage cells adapted to store the second parallel data received by the buffer,

a buffer controller adapted to cause the buffer to transmit an additional predetermined amount of the second parallel data when a number of the storage cells storing the second parallel data received by the buffer but not yet transmitted by the buffer is less than or equal to a first threshold,

wherein the buffer controller is further adapted to cause the buffer to delete a predetermined amount of the second words of the digital data when a number of the storage cells storing the second parallel digital data received by the buffer but not yet transmitted by the buffer is greater than or equal to a second threshold, and

a serializer adapted to convert the second parallel data transmitted by the buffer to second serial data, and to transmit the second serial data to the channel according to the second clock signal;

wherein the first and second clock signals are independent.

34. The SERDES of claim 33:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the second parallel data comprises one of the fill words.

35. The SERDES of claim 33:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the second parallel data that is deleted by the buffer comprises one of the fill words.

36. The SERDES of claim 33:

wherein the buffer comprises a plurality of storage cells adapted to store the second parallel data received by the buffer;

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

37. The SERDES of claim 33:

wherein the buffer comprises a plurality of storage cells adapted to store the second parallel data received by the buffer;

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

38. The SERDES of claim 33, wherein the buffer is a first-in first-out (FIFO) buffer.

39. The SERDES of claim 33, wherein the channel comprises a fibre channel.

40. The SERDES of claim 33, wherein the serializer is further adapted to transmit the serial data to the channel at a rate greater than or equal to 4 Gbps.

41. A storage area network (SAN) comprising the SERDES of claim 33.

42. A serializer/deserializer (SERDES) comprising:

deserialization means for deserializing data, the deserialization means comprising deserializer means for receiving first serial data from a channel, and for converting the first serial data to first parallel data; and

serialization means for serializing the digital data, the serialization means comprising

buffer means for receiving second parallel data according to a first clock signal, and for transmitting the second parallel data according to a second clock signal, wherein the buffer means comprises a plurality of storage cell means for storing the second parallel data received by the buffer means,

buffer controller means for causing the buffer means to transmit an additional predetermined amount of the second parallel data when a number of the storage cell means storing the second parallel data received by the buffer means but not yet transmitted by the buffer means is less than or equal to a first threshold,

wherein the buffer controller means causes the buffer means to delete a predetermined amount of the second parallel data when a number of the storage cell means storing the second parallel data received by the buffer means but not yet transmitted by the buffer means is greater than or equal to a second threshold, and

serializer means for converting the second parallel data transmitted by the buffer means to second serial data, and for transmitting the second serial data to the channel according to the second clock signal;

wherein the first and second clock signals are independent.

43. The SERDES of claim 42:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the second parallel data comprises one of the fill words.

44. The SERDES of claim 42:

wherein the second parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the second parallel data that is deleted by the buffer means comprises one of the fill words.

45. The SERDES of claim 42:

wherein the buffer means comprises a plurality of storage cell means for storing the second parallel data received by the buffer means;

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

46. The SERDES of claim 42:

wherein the buffer means comprises a plurality of storage cell means for storing the second parallel data received by the buffer means;

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

47. The SERDES of claim 42, wherein the serializer means transmits the serial data to the channel at a rate greater than or equal to 4 Gbps.

48. A storage area network (SAN) comprising the SERDES of claim 42.

49. An apparatus comprising:

a buffer adapted to receive parallel data according to a first clock signal, and to transmit the parallel data according to a second clock signal, wherein the buffer comprises a plurality of storage cells adapted to store the parallel data received by the buffer;

a buffer controller adapted to cause the buffer to transmit an additional predetermined amount of the parallel data when a number of the storage cells storing the parallel data received by the buffer but not yet transmitted by the buffer is less than or equal to a first threshold;

wherein the buffer controller is further adapted to cause the buffer to delete a predetermined amount of the parallel data when a number of the storage cells storing the parallel data received by the buffer but not yet transmitted by the buffer is greater than or equal to a second threshold; and

a serializer adapted to convert the parallel data transmitted by the buffer to serial data, and to transmit the serial data according to the second clock signal;

wherein the first and second clock signals are independent.

50. The apparatus of claim 49:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the parallel data comprises one of the fill words.

51. The apparatus of claim 49:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the parallel data that is deleted by the buffer comprises one of the fill words.

52. The apparatus of claim 49:

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

53. The apparatus of claim 49:

wherein the total number of the storage cells in the buffer is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

54. The apparatus of claim 49, wherein the buffer is a first-in first-out (FIFO) buffer.

55. The apparatus of claim 49, wherein the serializer transmits the serial data to a fibre channel.

56. The apparatus of claim 49, wherein the serializer is further adapted to transmit the serial data to the channel at a rate greater than or equal to 4 Gbps.

57. A storage area network (SAN) comprising the apparatus of claim 49.

58. An apparatus comprising:

buffer means for receiving parallel data according to a first clock signal, and for transmitting the parallel data according to a second clock signal, wherein the buffer means comprises a plurality of storage cell means for storing the parallel data received by the buffer means;

buffer controller means for causing the buffer means to transmit an additional predetermined amount of the parallel data when a number of the storage cell means storing the parallel data received by the buffer means but not yet transmitted by the buffer means is less than or equal to a first threshold;

wherein the buffer controller causes the buffer means to delete a predetermined amount of the parallel data when a number of the storage cell means storing the parallel data received by the buffer means but not yet transmitted by the buffer means is greater than or equal to a second threshold; and

serializer means for converting the parallel data transmitted by the buffer means to serial data, and for transmitting the serial data according to the second clock signal;

wherein the first and second clock signals are independent.

59. The apparatus of claim 58:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the parallel data comprises one of the fill words.

60. The apparatus of claim 58:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the parallel data that is deleted by the buffer means comprises one of the fill words.

61. The apparatus of claim 58:

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

62. The apparatus of claim 58:

wherein the total number of the storage cell means in the buffer means is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

63. The apparatus of claim 58, wherein the serializer means transmits the serial data to the channel at a rate greater than or equal to 4 Gbps.

64. A storage area network (SAN) comprising the apparatus of claim 58.

65. A method comprising:

storing parallel data according to a first clock signal;

retrieving the parallel data according to a second clock signal;

converting the retrieved parallel data to serial data;

transmitting the serial data according to the second clock signal;

wherein the first and second clock signals are independent;

transmitting an additional predetermined amount of the parallel data when a number of storage cells storing the parallel data stored but not yet retrieved is less than or equal to a first threshold; and

deleting a predetermined amount of the parallel data when a number of the storage cells storing the parallel data stored but not yet retrieved is greater than or equal to a second threshold.

66. The method of claim 65:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the parallel data comprises one of the fill words.

67. The method of claim 65:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the parallel data that is deleted comprises one of the fill words.

68. The method of claim 65:

wherein the total number of the storage cells available to store the parallel data is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

69. The method of claim 65:

wherein the total number of the storage cells available to store the parallel data is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

70. The method of claim 65, wherein the serial data is transmitted to a fibre channel.

71. The method of claim 65, wherein the serial data is transmitted at a rate greater than or equal to 4 Gbps.

72. A computer program embodying instructions executable by a computer to perform a method comprising:

storing parallel data according to a first clock signal;

retrieving the parallel data according to a second clock signal;

converting the retrieved parallel data to serial data; and

transmitting the serial data according to the second clock signal;

wherein the first and second clock signals are independent;

transmitting an additional predetermined amount of the parallel data when a number of storage cells storing the parallel data stored but not yet retrieved is less than or equal to a first threshold; and

deleting a predetermined amount of the parallel data when a number of the storage cells storing the parallel data stored but not yet retrieved is greater than or equal to a second threshold.

73. The computer program of claim 72:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the additional predetermined amount of the parallel data comprises one of the fill words.

74. The computer program of claim 72:

wherein the parallel data comprises a plurality of frames and a plurality of fill words; and

wherein the predetermined amount of the parallel data that is deleted comprises one of the fill words.

75. The computer program of claim 72:

wherein the total number of the storage cells available to store the parallel data is 11;

wherein the first threshold is 3; and

wherein the second threshold is 6 or 8.

76. The computer program of claim 72:

wherein the total number of the storage cells available to store the parallel data is 11;

wherein the first threshold is 3; and

wherein the second threshold is 10.

77. The computer program of claim 72, wherein the serial digital data is transmitted to a fibre channel.

78. The computer program of claim 72, wherein the serial data is transmitted at a rate greater than or equal to 4 Gbps.